

## GSM wireless reference design on a DSP/FPGA architecture

The Lyrtech GSM wireless reference design is a DSP/FPGA-based GSM reference design that showcases the powerful combination of a high-end DSP SOC, the Texas Instruments DM6446 DSP+ARM SOC (System-On-a-Chip), and Virtex4 FPGA and how it can be applied to software radio processing in an embedded wireless device. The reference design runs on the Lyrtech SFF (Small Form Factor) SDR DP (Development Platform), jointly developed with Texas Instrument and Xilinx.

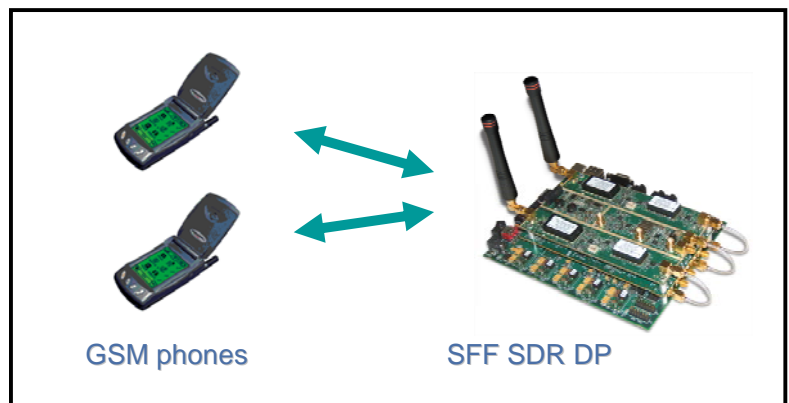
The reference design is a simplified GSM system that uses the Lyrtech GSM Base Station protocol stack and implements basic communication between 2 GSM devices and the SFF SDR DP that emulates BTS (Base Transceiver System) and network functions (see figure below). It provides most of layer-1 and layer-2 modules for the DSP and FPGA, while layer-3 modules are implemented for basic demonstration. A mixed design flow is used, where protocol layer targeted on the DM6446 are implemented in C/assembly, and physical layer on the FPGA, using a model-based design (MBD) tool flow.

The target platform is the modular SFF SDR DP, equipped with a baseband DSP/FPGA board, a high-speed sampling board used to sample the intermediate frequencies (IF) and a radio frequency (RF) front end. IF processing is done within the FPGA. Its design is implemented with Simulink and System Generator for DSP software tools.

Baseband processing is done by the DSP (see figure 1) using the Lyrtech GSM GSM Base Station protocol stack and DSP libraries. Layers 2 and 3 event-driven code runs on the DSP, but could be targeted on the companion ARM processor. A host application allows to monitor the BTS-emulation activity through an Ethernet link.

### Typical reference design demo setup

Two GSM Mobiles communicates via the SFF platform emulating a GSM BTS



#### Basic Features

- Perform call set-up and loopback between two GSM mobiles
  - Optionally, voice can be decoded and output locally (or to network)
- Implements ETSI GSM recommendations
  - Most voice-call related layer 1 and 2 messages and primitives
  - Subset of layer 3 Call Control messages
    - Allows BTS emulation and basic call establishment
- Targeted at Lyrtech SFF SDR DP
  - Based on TI DM6446 SOC DSP (ARM9 + C64x DSP) and Virtex 4 FPGA
  - Retargetable C-Code for protocol layers
    - Code is non-OS specific
    - Code runs on DSP or can easily be splitted between DSP and GPP
    - Uses 64xx assembly-coded Lyrtech GSM voice coding libraries
  - FPGA designed using Model-Based Design
    - Allows system simulation and verification
    - Can be easily retargeted at other FPGAs
  - SFF SDR platform is RF/IF/Baseband modularized, so it can be retargeted to customer specific technologies for IF and RF sections
- Applications:
  - Pico base stations
  - GSM monitoring systems
  - Advanced reprogrammable multi-mode/SDR handhelds
  - GSM-based sensors

Figure 1 illustrates the main components of the system, and illustrates the DSP/FPGA processing partition.

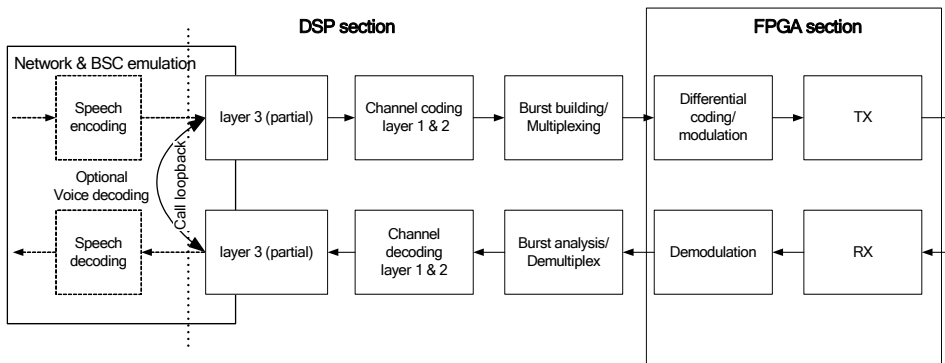


Figure 1 DSP/FPGA GSM partitioning, BTS emulation mode

### Baseband and protocol processing

Most layer 1 and 2 messages (mainly those oriented toward voice communication) are implemented, while a subset of layer 3 messages is implemented. Layer 3 implementation also realizes network function allowing a complete call set-up between two mobiles. Optionally, voice-oriented channels and voice coders/decoders necessary to GSM voice decoding are available for local audio output, using AMR coders implemented using Lyrtech DSP optimized C code libraries.

### Protocol layers

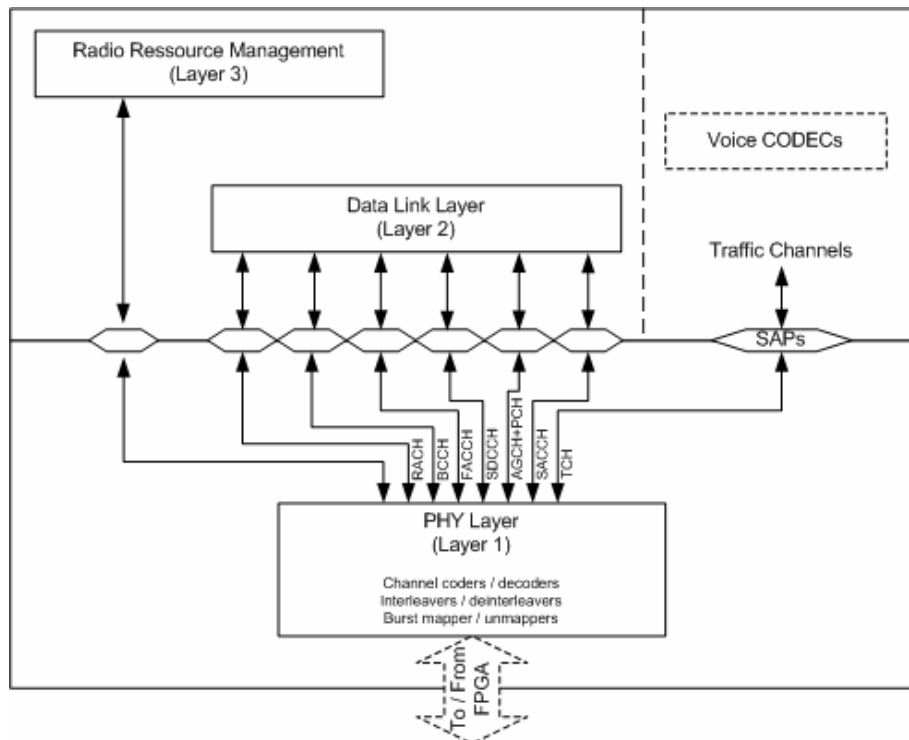


Figure 2 GSM Protocol layers

Layer 3 messages are partially implemented, and include the following main messages. ETSI recommended primitives are also used.

**Layer 3 subset:**

CALL CONFIRMED, CALL PROCEEDING  
CONNECT, CONNECT ACKNOWLEDGE, DISCONNECT  
RECALL  
SETUP  
ALERTING  
RELEASE, RELEASE COMPLETE  
CHANNEL REQUEST, RELEASE  
PAGING REQUEST, RESPONSE  
ASSIGNMENT COMMAND, COMPLETE, IMMEDIATE ASSIGNMENT  
CHANNEL MODE MODIFY, CHANNEL MODE MODIFY ACKNOWLEDGE  
START, STOP DTMF, ACKNOWLEDGE

**Primitives:** all inter-layer primitives are implemented

Layer 1-2 primitive:

MPH INFO

Layer 1-2 primitives:

PH DATA  
PH RA  
PH RA CONFIRM

Layer 2-3 primitives:

DL DATA  
DL UNIT DATA  
DL ESTABLISH  
DL RELEASE  
DL RANDOM ACCESS INDICATION

## Estimation of FPGA resources

Resources used in the Virtex 4 SX35 FPGA are approximately as follows: 60 % of logic slices, 30 % of BRAM and 20 % of DSP48 slices. The DSP design uses 20 % of the available DSP MIPS.

### Wireless reference design technical features and specifications (Rev. 4.0)

- IF and baseband processing of 900-MHz GSM bands
- Signal acquisition with ADACMaster III 105-MHz sampling capabilities
- IF I and Q heterodyning, down-sampling, up-sampling, and burst processing by FPGA
- Design available in System Generator for DSP
- Baseband demodulation in DSP
- GSM layers 1 and 2 code available (using ETSI recommended primitives)
- Simplified communication establishment protocol (layer 3)
- Standard OS-independent C-code
- DSP only version is available;
- Can optionally be partitioned between ARM GPP and DSP
- Uses Lyrtech GSM voice and channel coders DSP libraries for voice decoding
- RF front end (translates 900-MHz carrier signals to 70-MHz IF)
- Available as-is or as a basis for customisation
- See also the detailed specifications of the SFF SDR DP for more technical information on the RF, ADC/DAC and DSP/FPGA processing boards.

## Background

### Lyrtech quickly transforms customer ideas and concepts into products

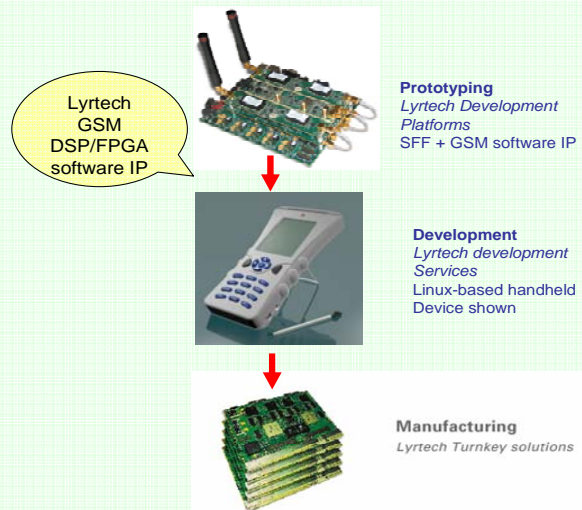
The Lyrtech SignalMaster development platform line of products, when combined with leading-edge MATLAB/Simulink tools, can be used at all stages of development projects: from early system simulations, through rapid prototyping and concept verification, to validation and preproduction.

Lyrtech also offers complete electronic design, prototyping, and manufacturing services in any field where complex DSP challenges arise.



### Use the Lyrtech “1-2-3 Go To Market” development advantage

- 1. Prototype:** Develop rapidly a working prototype using the SFF SDR DP and Lyrtech software IP.
- 2. Develop:** Move portable design code to your own final product or let Lyrtech provide a turnkey solution for you
- 3. Manufacture:** Use Lyrtech EMS capabilities for small-medium volume production, or select Lyrtech production partners for high volumes



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### ABOUT LYRTECH

In today's world, digital signal processing technology is vital to network and wireless communications, audio and video processing, as well as electronic systems in all fields of technology. Lyrtech has more than 20 years of experience in the delivery of advanced digital signal processing solutions to companies worldwide. Serving clients across the Americas, Asia, and Europe, Lyrtech offers a full range of DSP-FPGA development platforms, as well as design, prototyping, and manufacturing of electronic products. The company works in partnership with such industry leaders as Texas Instruments, The MathWorks, and Xilinx. Lyrtech delivers unsurpassed quality and support to its large OEM customer base, which includes many prestigious names such as BAE Systems, Defence Research and Development Canada (DRDC), the European Aerospace Defence and Space Company (EADS), Fujitsu, Harris, IIT, Motorola, Neural Audio, NTT DoCoMo, and Samsung-Thales.

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