

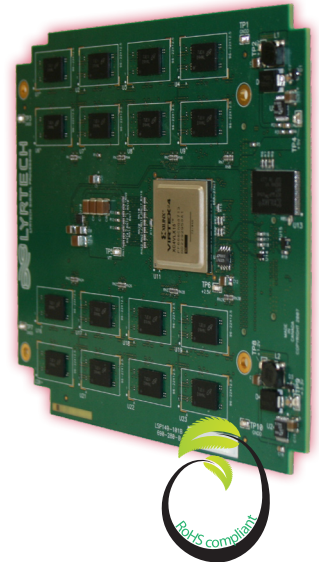
# Memory module

## Add-on for VHS-ADCs and VHS-DACs

The memory module offers an additional 2 GB of SDRAM to carrier [VHS-ADCs](#) and [VHS-DACs](#). When installed on a carrier board, its eight ADC or DAC channels can easily be recorded or played back at full rate (input 105 MSPS, output 480 MSPS). What's more, the FPGAs of VHS-ADCs and VHS-DACs can preprocess data before recording it through the selected channels of the module or post-process the data after playback from the module.

### Application fields

- Vector signal generators (VSGs) and analyzers (VSAs)
- MIMO test equipment
- Multichannel, high-speed instrumentation
- Medical imaging (PET, Gamma-ray detection)



### AT A GLANCE

- Total of 2 GB of SDRAM
- Record or play back at the maximum sampling rate from a carrier board's eight channels
- User-friendly interface and easy-to-use host API to access the memory
- Support for model-based design flow

### Software development tools

#### Memory module onboard FPGA application

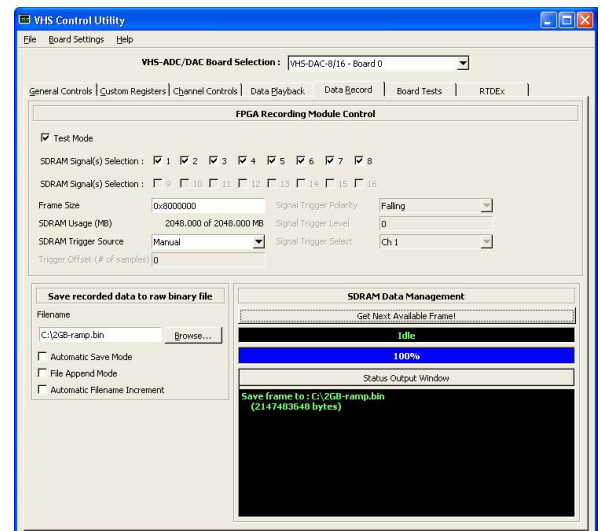
The memory module's flash PROM comes preloaded with an application that loads the FPGA logic of the module at startup. This application thoroughly manages and configures the module's SDRAM and allows the FPGA of the carrier board to simultaneously record to or play

back from up to the memory module's eight, 14-bit data channels.

**Note that the FPGA of the memory module cannot be targeted.**

### Communication and configuration from the VHS-ADC and VHS-DAC

The board software development kit (BSDK) and the model-based design kit (MBDK) of carrier VHS-ADCs and VHS-DACs include the software necessary to transfer data between a carrier's FPGA and the memory module. They also come with DSP and host APIs, FPGA cores (for BSDK users), and blocksets (for MBDK users) to control the memory module's parameters and the recording/playback channels. The software also includes a user-friendly interface to access the recorded or played back data.



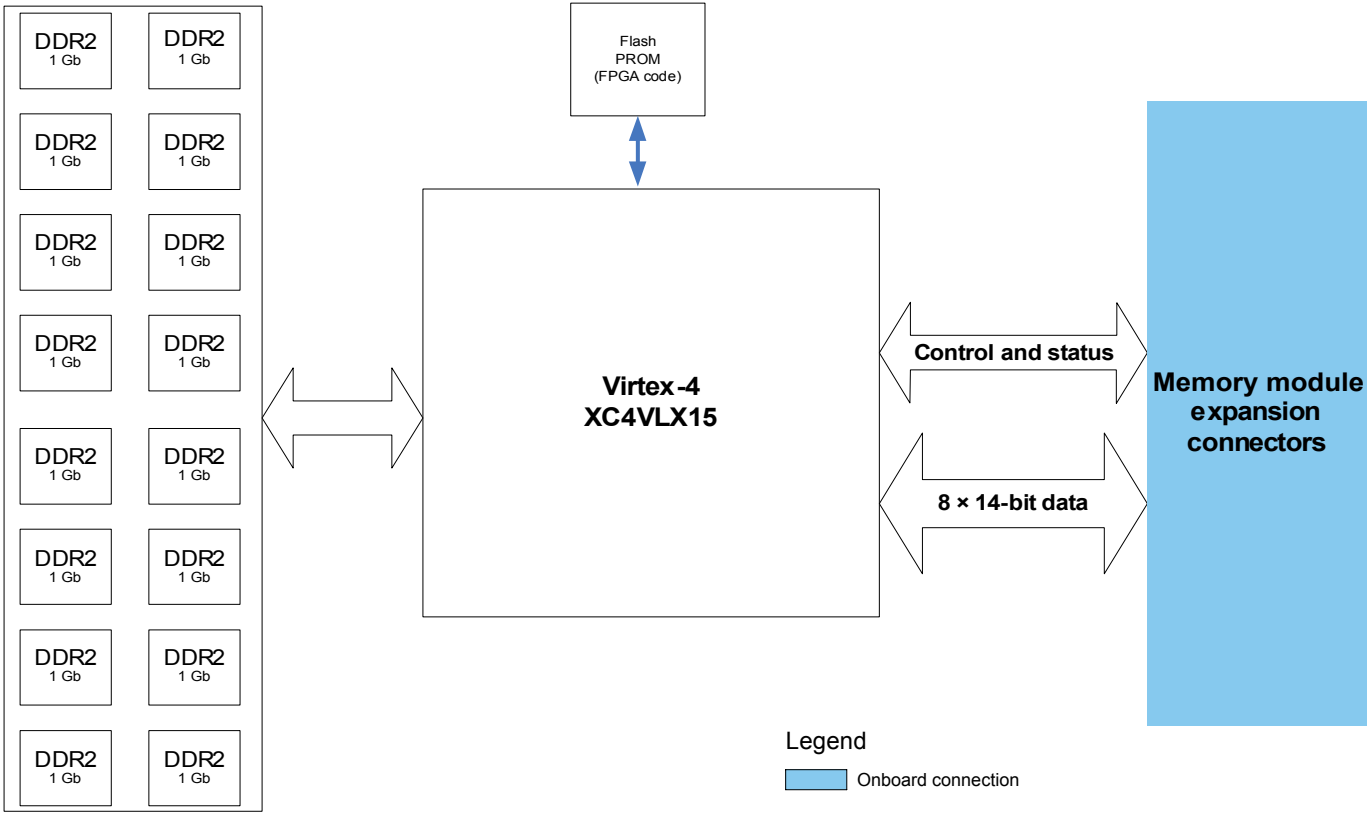
## Specifications

Recording/Playback channels	Simultaneously available 14-bit, user-selectable 1, 2, 4, or 8 channels
Transfer rate	125 MHz per channel
Capacity	2 GB
Trigger modes	<ul style="list-style-type: none"> <li>• Snapshots start on trigger event (single-shot or auto rearming)</li> <li>• Free-Running and stop on trigger event (single-shot or auto re-arm)</li> </ul>
Trigger sources	<ul style="list-style-type: none"> <li>• External (VHS-ADC or VHS-DAC external trigger)</li> <li>• From user VHS-ADC or VHS-DAC FPGA design</li> <li>• From selected recorded signal amplitude</li> <li>• From host controller cPCI CPU</li> </ul>

Recording/Playback example	Duration	Samples per channel
1 channel at 100 MHz	$\frac{2 \text{ GB}}{1 \times 2 \text{ bytes} \times 100 \text{ MHz}} = 10.737 \text{ s}$	$\frac{2 \text{ GB}}{2 \text{ bytes/sample}} = 1 \text{ gigasample}$
8 channels at 100 MHz	$\frac{2 \text{ GB}}{8 \times 2 \text{ bytes} \times 100 \text{ MHz}} = 1.342 \text{ s}$	$\frac{2 \text{ GB}}{2 \text{ bytes/sample} \times 8 \text{ channels}} = 128 \text{ megasamples}$

Note that each 14-bit sample uses 2 bytes of memory.

## Block diagram



### FOR MORE INFORMATION

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