

Flexible DSP-Platform for Rapid Prototyping

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Abstract

Due to the ever growing need for faster processing of algorithms the field of DSP applications have grown significantly during the last few years. Digital signal processing is not only being used in both the classical field of multimedia (e.g. audio and video processing) but also in industrial applications (e.g. control algorithms for power converters). Thus, a suitable and very flexible development platform for prototyping of these applications is needed.

Currently, development boards tend to be very application specific. They do not provide the developer with enough flexibility. Processor, memory and interfaces are chosen according to the particular demands. For each application a new hardware prototype is designed, which is time consuming and expensive. This contradicts the rapid prototyping concept.

This paper describes a reference design for a multi application platform that is flexible enough to serve as the core module of any DSP application in research and development. It provides a powerful processor, lots of memory, multiple standard interfaces and the ability to be expanded easily.

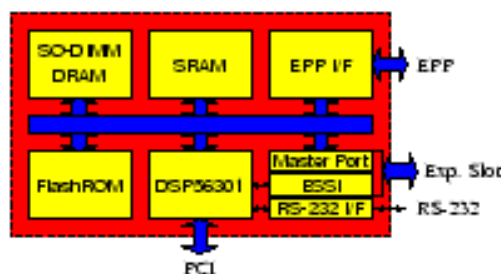


Figure 1: DSP Module PC-Eye1

1 Overview

A reference design called PC-Eye1 was realized. Its structure is illustrated in fig. 1. It is based on the Motorola DSP56301 and provides extensive memory, various standard interfaces (i.e. PCI, RS-232, EPP), and an universal expansion slot, that consists of two fast synchronous serial interfaces (ESSI) and a Master Port as a DSP bus extension. A flexible power supply enables the board to work as PCI plug-in card or as a stand-alone module.

The included software support eases the development effort and allows the DSP developer to concentrate on his design goal.

2 DSP

The general purpose DSP56301 from Motorola was the chosen processor for PC-Eye1 because of its high degree of flexibility paired with powerful technical features.

This DSP is unique to the DSP market, because of its integrated PCI controller. When designing a hardware platform with PCI plug-in facilities no additional hardware effort is required. Two very fast synchronous serial interfaces (20 MBit/s each) and one (a)synchronous serial interface (10 Mbit/s) enable glueless connection to codecs (e.g. audio processing) and other peripheral I/O devices. Three on-chip timers for counting events and controlling various devices (e.g. power switches in PWM mode) together with the 6 channel DMA controller add to the power of the DSP.

The DSP contains 4 K-Words of internal program RAM and 4 K-Words of internal data RAM. The ALU incorporates a barrel shifter

that is suitable for bit stream processing (e.g. MPEG). 56 bit accumulators and rounding arithmetic provide a high accuracy for all calculations. Within a single clock cycle the DSP56301 executes up to 3 instructions and 6 DMA operations in parallel. The nominal clock rate can be 80 MHz or even 100 MHz. The system clock is very versatile because of the incorporated PLL. It allows a broad frequency range from a few Hz to over 100 MHz. Special bit manipulation and test commands allow the processor to perform classical controller tasks.

The DSP contains an on-chip emulator (OnCE™), that allows direct access to the processor and is used for PC or workstation based hardware debugging during development.

The structured way the processor has been built enables a realistic estimation of processing time and makes programming in assembler language easier.

3 PCI and Stand-Alone Operation

PC-Eye1 is a PCI plug-in card because of the integrated PCI interface on the DSP56301. The data transfer rate of the PCI bus is 132 MByte/s with a 32 bit word length at a clock frequency of 33 MHz. The DSP56301 is currently the only DSP with a PCI controller on-chip giving the PCI bus both master and slave ability. Thus this reference design is suitable for applications with the need for high speed data channels (e.g. video processing). The board can work in a 3.3 V and 5 V PCI environment.

A flexible power supply enables it to run as a stand-alone system. In this case, the PCI connector can be used for parallel general purpose I/O.

4 Memory Options

The board has external memory in addition to the internal DSP memory. A FlashROM with a maximum size of 256 kByte can be used for the storage of an initial operating system, loadable applications and data. Up to 2 M-Words fast SRAM for program and data storage support the DSP high performance processing abilities. The on board SO-DIMM socket enables additional memory extension of up to 8 M-Words DRAM. The overall maximum memory size is greater than 30 MBytes and more than sufficient for most DSP applications. The board's memory map is illustrated in **fig. 2**.

5 Standard Interfaces

In addition to the PCI interface the board contains standard interfaces such as a RS-232 and an EPP interface.

The RS-232 interface corresponds with the minimum requirements of the RS-232 standards that have been extended by RTS/CTS handshaking. The interface is internally connected with the serial communication interface (SCI).

The EPP interface is a compatible master and slave capable I/O port with a data rate of 5 MByte/s. When in EPP master mode it can communicate with PC peripherals. While running as a slave the data exchange operations can be controlled by a PC. The control and monitoring of the interface is done using external I/O registers. The programming model is identical to the internal DSP peripherals.

6 Expansion Slot

The Expansion Slot allows developers to extend the board with I/O modules of their choice (**fig. 3**). The interface specification is straightforward and a minimal effort is required for the development and integration of additional I/O

\$FFFFFF	Y: External IO-Register
\$FFFF80	X: Internal IO-Register
\$FFFF7F	
⋮	Free
\$D80000	
\$D7FFFF	
⋮	reserved for extra FlashROM
\$D10000	
\$D0FFFF	
⋮	FlashROM (8 bit)
\$D00000	
\$CFFFFFF	
⋮	reserved for extra SRAM
\$C20000	
\$C1FFFF	
⋮	SRAM (24 bit)
\$C00000	
\$BFFFFFF	
⋮	(DRAM, optional (24 bit))
\$400000	
\$3FFFFFF	
⋮	Free
\$001000	
\$000FFF	
⋮	Internal P-RAM (24 bit)
\$000800	
\$0007FF	
⋮	Internal XY-RAM (24 bit)
\$000000	Internal P-RAM (24 bit)

Figure 2: Memory Map

modules (i.e. A/D converters, audio codecs, digital I/O). The Expansion Slot is a key feature of the module. It allows the development platform to be easily adapted according to specific application requirements.

The Expansion Slot is divided into a 'Master Port' and an 'ESSI Port'. The 'ESSI Port' provides both ESSI interfaces of the DSP56301 (20 MBit/s each) to enable glueless connection

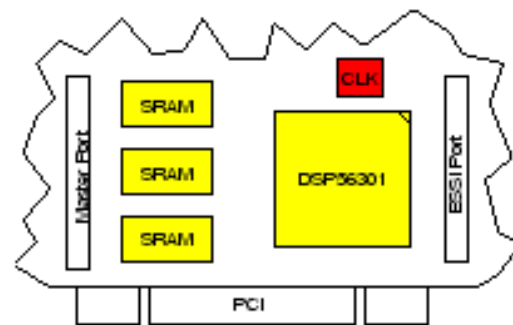


Figure 3: Expansion Slot

of serial A/D and D/A converters.

The 'Master Port' can be configured for two operation modes. The port consists of 5 bit addressing, 2 pre-coded chip select pins and 1 interrupt pin or 4 bit addressing and 4 pre-coded chip select pins. Additionally, it provides a read and write strobe signal. Thus, it is a full DSP bus extension. As shown in the memory map fig. 4, I/O registers are automatically mapped to the external I/O space of the DSP56301. Using the development software (chap. 8.2) they are addressed relative to symbolic base addresses.

\$FFFBF	Expansion Area C	IO_Base_C
⋮		
\$FFFFA0	Expansion Area A	IO_Base_A
\$FFF9F		
⋮		
\$FFF80		

Figure 4: Memory Map of Master Port

7 Status Display and Watchdog

Eight fixed LEDs display the operation status of the board (e.g. power failure, RS-232 and EPP status). The other eight LEDs can be controlled by software and are very useful for testing and debugging.

An intelligent watchdog controls the bus signals and user programmable signals. It is automatically deactivated during debug access by the host PC.

8 Software Support

One of the most time consuming tasks when developing DSP applications is the design of routines for system initialization and testing. The included initial operating system software DSPios Light handles this difficult part.

Software implementations using high level languages (e.g. C) are easy to maintain and portable, but they do not have the runtime efficiency of pure assembler code. The included development software MEPEE Light allows both good maintainability and high runtime efficiency.

8.1 Initialization Software

The initial operating system DSPios Light [3][5] supports the complete separation of the system initialization, test and application software, thus allowing hardware independent software development and easy stand-alone operation of applications. On boot-up, it performs a full initialization of the DSP and peripherals. It performs extensive system tests, additionally allows the automatic start of applications and enables booting from RS-232 and PCI. After application start-up, the system software frees all system resources and uses no system resources during run-time.

8.2 Development Tool

The programming environment MEPEE Light [4][6] is an assembler precompiler. It enables fast and extremely reliable development of DSP applications. It places special value on high maintainability and programming efficiency which result in a significant reduction in development effort. The binary code that is produced is identical to extremely optimized assembler code that would otherwise require great effort to program without this tool.

8.3 Template Applications with I/O-Handler

The development tool MEPEE Light contains examples of I/O handling (i.e. EPP, SPP, PCI, SCI) with the hardware platform. A software engineer can easily use them as templates for his own applications, because of the modular software concept. This also contributes to the rapid prototyping concept, because the developer can focus on his particular application goal.

8.4 Debugger

Tools from Motorola and third parties can be used for application development and debugging of the hardware board. They can use hardware debugging via the DSP OnCE™ interface.

The module is also supported by software debugging tools, which are designed for special purposes like real-time multi-tasking environments (e.g. "TORNADO for DSP" by Wind River Systems) enabling integration into a complete workbench for embedded applications using sophisticated GUIs.

9 Application Example

A good example of application development within the scope of the rapid prototyping concept is an Exhibition Guidance System. This project requires high processing performance, low power consumption and rapid prototyping according to the customer's requirements for a digital audio compression system.

The reference design PC-Eye1 was used for the prototyping of a model series (see fig. 5). As a universal hardware platform, the reference design is capable of handling the extensive external expansions such as Audio-IO, RF-Receiver, position identifier and keyboard interface. All signal processing for two different compression algorithms and control functions are handled by the DSP.

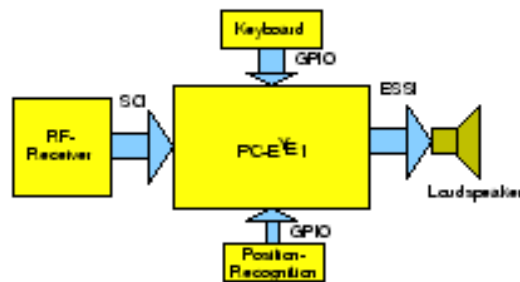


Figure 5: System Development using PC-EYE

The development of both additional hardware and software can be carried out in parallel during project time. Using the development tool MEPEE the application software of the module is strictly usable on the destination hardware. This means that after only 4 months of development a prototype of the Guiding System was developed.

10 Conclusion

A flexible reference platform for a broad application range within the field of signal processing has been developed. This flexible reference design is suitable as an OEM module or for rapid-prototyping because of its extensive interfaces, its easy extension and its transparent modular concepts.

The combination of hardware module and software takes routine work off the user, aids structured development of reliable maintainable and non-the-less powerful DSP applications. The potential user can concentrate on the research problem or development of product applications. This module can play an important role in rapid prototype designs in the field of DSP applications.

References

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